

REMARKS

This responds to the Advisory Action mailed on April 28, 2005.

Claims 21, 28, and 34 are amended; as a result claims 21-40 are now pending in this application.

§112 Rejection of the Claims

Claims 34-40 were rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. The Advisory Action states that this rejection has been withdrawn, but the Applicant notes that the Examiner did not enter the amendment made in the Response to Final for claim 34. Applicant assumes that this means the arguments presented were sufficient independent of the amendment to overcome this rejection. However, with this amendment and response being accompanied with an RCE, the original amendments to claim 34 that were not entered have been reasserted here. Therefore, under either interpretation the Applicant believes that this rejection has now been sufficiently overcome and has been withdrawn.

§102 Rejection of the Claims

Claims 21-24, 26-32 and 34-40 were rejected under 35 USC § 102(b) as being anticipated by Macon, Jr. et al. (U.S. 5,600,817). It is of course fundamental that in order to sustain an anticipation rejection that each and every step or element in the rejected claims must be taught or suggested in the cited reference.

Applicant asserts that Macon always performs a prefetch into cache for each piece of data. In support of this, Applicant directs the Examiner to column 5, lines 58-67 of Macon. Here, it is stated that “[a]t block F a determination is made if the MRRS HIT is the first HIT to the MRRS 7a . . . [i]f NO, indicating that the MRRS 7a has been HIT at least once before by a previous DADDR, control passes to Block O to EXIT . . . [t]hat is, no prefetching occurs . . . [a]s a result, only one prefetch I/O operation occurs for a given MRRS 7a entry.” Emphasis Added. This demonstrates Applicant’s position, which is that Macon always performs at least one prefetch for a given entry. *Emphasis Added.*

AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/659,920

Filing Date: September 11, 2003

Title: ADAPTIVE PREFETCH OF I/O DATA BLOCKS

Assignee: Intel Corporation

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Dkt: 884.A31US2 (INTEL)

Conversely, Applicant's amended independent claims now positively recite that for at least some blocks prefetching does not occur. Macon does not make this distinction or include this limitation, since Macon is directed to delivery of all data from a cache.

Therefore, Applicant respectfully request that the rejections with respect to Macon be withdrawn and that the claims be allowed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joseph Mehrle at 513-942-0224, or the undersigned attorney to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By his Representatives,

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Date May 18, 2005

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18th day of May 2005.

John D. Gustav-Worthall

Name

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Signature